Fully Differential Two Stage Amplifier with Common Mode Feedback

A fully differential amplifier is the most commonly used custom designed amplifier. The differential output gives you twice the output swing range that can be accomplished by a single ended amplifier with the same supply voltage. The amplifier design presented also has a cascoded first stage. This cascoded first stage allows for a dramatic improvement in the amplifier’s gain. A simple common source amplifier is used in the second stage in order to achieve a large output swing range. The amplifier design specifications were given as follows:

\[ V_{DD} = -V_{SS} = 2.5v \]

Total Power < 3mW (Including everything)

\[ SR \geq 30 \frac{V}{\mu s} \]

DC Gain ≥ 90dB
Gain Bandwidth Product (GBW) ≥ 25MHz
CMRR ≥ 100dB
Output swing cover 75% of \( V_{DD} - V_{SS} \)
Input Common Mode Range (ICMR): \( \text{ICMR} \geq 50\% \times (V_{dd} - V_{ss}) \)
Maximum overshoot for 0.1 V step response with gain of \( -1 \) resistive feedback <25%
Settling time in 0.5 V step response with gain of \( -1 \) resistive feedback: \( \leq 100 \) nS for \( \pm 0.1\% \).

CL=2pF

Design
The amplifier was designed with a cascoded differential first stage and a common source second stage. An overview of the entire design is given in figure 1 and the schematic of the amplifier topology is given in figure 2. The common mode feedback, used to keep the common mode output low was designed using a low gain amplifier to control the first stage current source. A resistive common mode feedback detection circuit was used. The common mode circuit design is shown in figure 3. The amplifier was biased using the previously designed Vdd independent current source and 5 voltage bias generators. The biasing circuitry design is shown in figure 4.
Figure 1: Design Overview

Figure 2: Amplifier Topology
I started by budgeting both the first and second stage currents. These currents were budgeted using the slew rate and power requirements. First of all the bias current of each of the 5 voltage bias generators was selected to be 10 µA for easy mirroring from the Vdd independent current source. This leaves the following power to be used in the two stages of the amplifier:

\[
P_{\text{total}} < 3mW \quad I_{\text{total}} < \frac{3mW}{5v} = 600\mu A \\
I_{\text{biasing}} = I_{\text{src}} + I_{v \text{ generators}} = 50\mu A \\
I_{\text{amp}} < 550\mu A
\]
Also, there is 10\(\mu\text{A}\) needed for the \(V_{\text{el2}}\) bias circuit giving \(I_1 = 50\mu\text{A}\)

\[
SR^+ \leq \frac{I_2}{C_{\text{Ltot}}} \quad I_2 \geq SR^+ \cdot C_{\text{Ltot}} = \left(30 \frac{V}{\mu\text{A}}\right) \cdot (4p\text{F}) = 120\mu\text{A}
\]
\[
SR^- \leq \frac{I_1}{C_C} \quad I_1 \geq SR^- \cdot C_C = \left(30 \frac{V}{\mu\text{A}}\right) \cdot (1p\text{F}) = 30\mu\text{A}
\]

Choose: \(I_1 = 40\mu\text{A}\) \(I_2 = 130\mu\text{A}\)

Next the sizing of each transistor needed to be chosen:

\[
\frac{W_1}{L_1} = \frac{W_2}{L_2} = \frac{W_{1c}}{L_{1c}} = \frac{W_{2c}}{L_{2c}} = \frac{2(20\mu\text{A})}{(40\mu\text{A})(0.1v^2)} = 10 = \frac{15\mu\text{m}}{1.5\mu\text{m}}
\]
\[
\frac{W_3}{L_3} = \frac{W_4}{L_4} = \frac{W_{3c}}{L_{3c}} = \frac{W_{4c}}{L_{4c}} = \frac{2(20\mu\text{A})}{(120\mu\text{A})(0.1v^2)} = \frac{10}{3} = \frac{5\mu\text{m}}{1.5\mu\text{m}}
\]
\[
\frac{W_7}{L_7} = \frac{2(50\mu\text{A})}{(40\mu\text{A})(0.2v^2)} = 4.2 = \frac{6.3\mu\text{m}}{1.5\mu\text{m}}
\]
\[
\frac{W_6}{L_6} = \frac{130\mu\text{A}}{(40\mu\text{A})(0.2v^2)} = 12.5 = \frac{30\mu\text{m}}{2.4\mu\text{m}}
\]
\[
\frac{W_5}{L_5} = \frac{13\mu\text{m}}{3 \frac{W_6}{L_6}} = \frac{13\mu\text{m}}{2.4\mu\text{m}}
\]
\[
\frac{W_{11}}{L_{11}} = \frac{W_{b11}}{L_{b11}} = \frac{2(10\mu\text{A})}{(40\mu\text{A})(0.2v^2)} = 2.5 = \frac{3\mu\text{m}}{1.2\mu\text{m}}
\]
\[
\frac{W_8}{L_8} = \frac{2(20\mu\text{A})}{(40\mu\text{A})(0.2v^2)} = 1.67 = \frac{2.5\mu\text{m}}{1.5\mu\text{m}}
\]

**Implementation**

After I had sized each transistor in the design I began to run some tests, however I soon discovered that the design had outputs that would saturate to Vdd. After further investigation I realized that I had a problem balancing the current in my upper PMOS circuits and the current being driven by the lower NMOS circuits. I also had a common mode feedback circuit that was both a gain and a gain-bandwidth product that were too high, causing the CMFB to be too fast.

I proceeded to correct the current imbalance in the amplifier’s two stages. The output of each stage was set to its nominal value, 0 for the first stage and to ground for the second stage. The common mode feedback was set to act nominally with a 0 common mode reading. The schematic of the current balancing is shown in figure 5.
Adjustments were made to the CMFB to lower the GB and then we ended with the following design parameters:

\[
\begin{align*}
\frac{W_1}{L_1} &= \frac{W_2}{L_2} = \frac{W_{1c}}{L_{1c}} = \frac{W_{2c}}{L_{2c}} = 35\mu m \\
\frac{W_3}{W_4} &= \frac{W_{3c}}{W_{4c}} = \frac{1.5\mu m}{13\mu m} \\
\frac{W_7}{2(50\mu A)} &= \frac{L_7}{L_{3c}} = \frac{6.3\mu m}{1.5\mu m} \\
\frac{W_6}{L_6} &= \frac{(40\mu A)(0.2v^2)}{130\mu A} = \frac{12.5}{30\mu m} \\
\frac{W_5}{L_5} &= \frac{1}{3} \frac{W_6}{L_6} = \frac{13\mu m}{2.4\mu m} \\
\frac{W_{11}}{L_{11}} &= \frac{W_{b11}}{L_{b11}} = \frac{2(10\mu A)}{(40\mu A)(0.2v^2)} = \frac{2.5}{3\mu m} \\
\frac{W_8}{L_8} &= \frac{2(20\mu A)}{(40\mu A)(0.2v^2)} = \frac{2.5\mu m}{1.5\mu m}
\end{align*}
\]

Also the following parameters were choosen:

**Test bench Results**

*DC gain, Gain-bandwidth product, and phase response*
The first test ran was to ensure the DC gain and gain-bandwidth product requirements of 90 dB and 25 MHz, respectively, were meet. Then the same test bench was used to characterize the system’s phase response. We were able to achieve a DC gain and gain-bandwidth very close to the specifications. The DC gain was 90.51 dB and the GB was 26.37 MHz. Although initially the DC gain was higher than the specifications, the gain was reduced to save area. These measurements are shown in the plot of the frequency response of the gain in figure 7. The phase is characterized in figure 8.

Figure 6: Test bench for measuring the DC gain, gain-bandwidth product, and the open-loop phase response.
Figure 7: Bode plot of the frequency response of the gain

Figure 8: Bode plot of the frequency response of the phase
Total Power

Current Budget:
Total Current: $I_{total} = 417.4\mu A$

Amplifier: First stage $I_1 = 49.18\mu A$  Second stage $I_2 = 2 \times (130.5\mu A) = 261\mu A$

CMFB: $I_{CMFB} = 19.4 \mu A$  Amplifier Total: $329.58 \mu A$

Biasing: $I_{I_{src}} = 20.02 \mu A$  $I_{v_{bias}} = 4 \times (10.02\mu A) + 27.79\mu A = 67.87\mu A$

Biasing Total: $I_{biasing} = 70.12\mu A$

Total Power

$$P = (417.4\mu A)(5V) = 2.087\, mW$$

Output Swing Range

The output swing range was measured using the test bench shown in figure 6

![Output Swing Range Test Bench](image)

Figure 9: Output Swing Range Test Bench

As shown in figure 10, the output swing range has met the design specifications
Figure 10 Output Swing range test result

**CMRR**

The CMRR was measured using the same test bench in Figure 6: Test bench for measuring the DC gain, gain-bandwidth product, and the open-loop phase response.

The DC common mode gain is -34.38 dB, which means that the CMRR for this amplifier is 124.9 dB, greater than 100 dB requirement.
ICMR

The ICMR test bench is the same as in Figure 6: Test bench for measuring the DC gain, gain-bandwidth product, and the open-loop phase response.

The ICMR test results are shown in figure 12 below.
As shown above the ICMR is 3.295 V, which exceeds the design specifications.

**Overshoot and Settling time**

The overshoot and settling time test use the same test bench with different input amplitude.

As shown in the above figure, the maximum overshoot is 9.33%, which meets the design specifications.
As shown above, the settling is 73 ns, which also meets the design specifications.

**Slew Rate**

Next the slew rate was tested using the test bench shown in figure 8. The input was slewed using a large step input. The slew rate was found to be $58.5 \frac{V}{\mu s}$. However there is also a nonlinearity in the data around half way through the slewing step output.
Figure 16: Slew rate test bench

Figure 17: Slew rate results
Conclusion
In this lab, we have successfully designed and tested a two stage differential operational amplifier, which meets all the design specifications. From Slew rate specifications, current at each stage can be determined. From selected $V_{eb}$ and phase margin specification, the preliminary sizes of the transistors can be determined. After preliminary design is simulated, sizes of the transistors are modified to ensure proper CMFB bandwidth, enough phase margins, and enough differential gain, differential bandwidth. Trade off must be made between total power consumption, the total area and performance of the amplifier. Over engineering are avoided. Various test benches are developed to test required design specifications. From this lab, we have learnt the basic design procedure for operational amplifier, which requires almost all previous learnt knowledge. The idea of trade off between circuits parameters are also carried out in the lab.