Georgia Institute of Technology

DEPARTMENT OF ELECTRICAL AND COMPUTER ENGINEERING

ECE-6414: Analog Integrated System Design – Spring 2013

4:35pm – 5:55 pm, Tue, Thu, Instructional Center 213

http://www.ece.gatech.edu/academic/courses/ece6414/S13

Instructor: Maysam Ghovanloo, Ph.D. (mgh@gatech.edu), Phone: (404) 385-7048

Office Hours: Fridays 2:00-4:00 pm, other times with prior appointment

Co-Instructor: Mehdi Kiani (m_kiani@gatech.edu), Wednesdays 2:00-4:00 pm

Textbooks: R. Jacob Baker, *CMOS Circuit Design, Layout, and Simulation* (3rd edition), IEEE & Wiley, 2010. ISBN 978-0-470-88132-3

P.E. Allen and D.R. Holberg, *CMOS Analog Circuit Design* (2nd edition), Oxford U. Press, 2002. ISBN13: 9780195116441

Other References: (recommended)

1. Analysis and Design of Analog Integrated Circuits, 5th ed.
   P. Gray & Meyer
2. Design of Analog CMOS Integrated Circuits
   B. Razavi
3. The Art of Analog Layout, 2nd ed.
   A. Hastings
4. Analog Integrated Circuit Design
   D.A. Johns and K. Martin

Prerequisites: Analog Electronics (ECE-4430 and 3050 or equivalent), Co-requisites: None

It is assumed that you are familiar with the following topics:

1. Circuit theory, frequency response, small signal modeling and analysis
2. Solid-state devices and microelectronic circuits: P-type and N-type semiconductors, PN junctions, bipolar junction transistors, and MOS field-effect transistors (MOSFET).
3. Analog circuit building blocks such as current mirrors, reference generators, single and multi-stage amplifiers, differential amplifies, and OpAmps.
4. Knowledge of MATLAB and available CAD tools such as SPICE or Cadence.

Course Description:

After a brief review of the prerequisites, we will look at some of the more advanced analog building blocks such as fully-differential OpAmps and dynamic analog circuits. We will use analog IC building blocks to construct simple analog IC systems such as data converters, filters, mixers, etc. We also review the characteristics and specifications of such analog and mixed-mode circuits from the system design perspective. This course is highly design/project oriented and emphasizes on intuitive understanding of circuits, particularly those topics used in analog

ASIC design. As such, it requires sufficient time to be spent on understanding the course materials and applying them to the course projects. However, this course will provide you with valuable hands-on experience as you go through a real analog ASIC design cycle from circuit idea and specifications to a layout ready for tapeout. Organization, attention to the details, engineering compromise, optimization, time management, and teamwork will also prove to be important in analog integrated system design.

Topical Outline:

Introduction, Review of analog IC building blocks

Noise analysis in analog circuits

Advanced current mirrors, amplifiers, and filters

Switched-capacitor circuits

Fully differential and high performance OpAmps

High speed comparators

Digital-to-analog converters (DAC)

Analog-to-digital converters (ADC)

Nonlinear analog circuits and mixers

Project Timeline:

Course Project:

Groups of three students should choose an analog system of their choice using a variety of the major analog and mixed-mode circuit blocks to be discussed in this course, preferably for a particular application in bioengineering or life sciences. Occasionally it would be acceptable for two or even three teams to each work on a sub-system of the larger analog system, provided that there would be a sufficient variety of analog building blocks in each sub-system. Teams are encouraged to consult with the instructor in choosing their topics. Each team proposes their project topic in a 2-page draft by Draft-1 deadline (about 4 weeks through the semester). Draft-1 should include a rough block diagram of the analog system showing the inputs and outputs of each block, as well as the entire system. It should also include a brief description of the biomedical application and any relevant online or published references that the group might have visited along with sufficient design specifications for each block. It should also indicate the tentative role and responsibilities of each team member. Each team should select one of the members as the main point of contact with the instructor. A separate page can be dedicated to the list of references that the group has found and studied to come up with the project idea (do not include a reference unless you have read it).

After receiving approval from the instructor, team members perform a thorough literature search on their selected topic, and come up with more specific analog ASIC design ideas for the building blocks, detailed specifications, and the functions that they would serve in the system

and eventually for the selected application. A summary of the literature survey, a detailed system block diagram, selected circuit topologies, and design targets for each block should be included in a 2nd Draft, and turned in by Draft-2 deadline (about 6 weeks through the semester). The page limit for Draft-2 is 7 pages including all figures but not references. System level simulations using ideal circuit components in Cadence, MATLAB, Simulink, or any other CAD tool is highly encouraged at this stage to demonstrate the functionality of the main idea, identify potential challenges, and also guide the team towards a more accurate estimation of the required specs for each building block.

Please note that ECE-6414 does not include any CAD tool training. In case you do not have sufficient prior background in using CAD tools, particularly Cadence, please make sure to go through online tutorials and consult with the other team members. Draft-2 should include a table summarizing the "Design Specifications", including the desired design targets. It can also include a column showing the simulation results up to that point. The instructor will provide each team with individual feedback on Draft-2.

At this stage, team members start/continue implementing their ASIC designs at the detailed transistor level, including layout, using Cadence tools. All ASIC designs should use the ON Semiconductor 0.5-µm standard CMOS process (C5N). Detailed information about this process and transistor models are available through MOSIS website (www.mosis.com/on_semi/c5/). This process operates reliably in 3-5V supply range. Using low voltage circuit design techniques, operation at lower voltages is also possible.

Considering the significance of ASIC layout in the performance of analog circuits, important layout design techniques that affect the circuit performance in terms of matching, minimizing parasitic components, and linearity, will be covered in class. The entire proposed circuit/system should be laid out, following these layout design guidelines. Part of the project grade is dedicated to the quality of layout and post-layout simulations. Your entire layout, including pad frame and protection circuitry should fit within half of a MOSIS "Tiny Chip", which means 1500 x 750 μm^2. Every two teams will be sharing one 1.5 x 1.5 mm^2 Tiny Chip.

There will be a Design Review about 6 weeks after Draft-2, when all circuit schematics at transistor level should be complete and simulated. The instructor will review the simulation results for each design along with the team members at a computer station and provide them with feedback. Part of the simulation results will be graded at this stage.

The team members will have a chance to modify and improve their circuit designs during the last month of the semester as they layout their designs and observe the performance of their circuit blocks more realistically in post-layout simulations.

All the schematic modifications, simulations, and layouts have to be completed by the last day of classes, which is indicated as the "Post-layout Simulation" date on the course schedule. The instructor will hold a second design review on that day and review the layouts and post-layout simulations with the team members. The top-level schematic and layout of the ASIC design should pass design rule check (DRC) and layout vs. schematic (LVS) test.

Finally by the end of the semester each team will turn in a report that should follow the *IEEE standard journal format* (http://www.ieee.org/documents/TRANS-JOUR.doc). This paper should include a summary of the literature survey, complete design, design theory and calculations, complete circuit schematics, circuit layout, pin-out diagram, post-layout simulation waveforms,

testing and measurement procedure (assuming the chip has been fabricated), and a table summary of the circuit characterization results (through post-layout simulations). Links to the IEEE general information for authors is provided on the course webpage. There, you can also find template files for MS-Word. The page limit for your final paper is 10 pages, excluding the list of references. This is the portion of the paper that will be graded based on completeness and quality of your writing. However, each team can add an unlimited number of appendixes to fully document their work.

During the final exam, each group should present the entire project in a 15-min slide presentation (~15 slides) for the rest of the class in a conference style. This session will be open to the public audience. Other faculty members and/or senior graduate students might be invited to evaluate the projects. The entire group should participate in the presentation and will be asked questions for 5-min by the instructor and other audience after their presentation.

To assess the individual participation of the team members, each member of the team will be asked to fill out an individual effort assessment form about the other team members.

Those teams with the best functional circuit designs, based on post-layout simulations and other performance measures, will be given a chance to further complete their ASIC designs and submit their layouts through MOSIS Educational Program (MEP) for fabrication. The actual tapeout date, according to the MOSIS schedule for the ON-Semi 0.5-µm process, is going to be 7/15/13 (https://www.mosis.com/db/pubf/fsched?org=ON-SEMI&year=2013).

The fabricated chips are expected to be back by mid Oct. 2013. Team members are encouraged to fully test and characterize their ICs after fabrication. Functional devices will be considered for additional experiments in their particular biomedical applications. If successful, measurement and experiment results can potentially be considered for submission to a professional conference.

Here are some further important details about the projects:

- You may discuss questions in large groups, but each person must independently perform and answer questions related to the entire project work. Therefore, the grading will not be the same among all members of each group.
- For the final presentation you should describe the background for your system (literature search results), state-of-the-art, methods, simulation results, challenges, and solutions. One should use fonts that can be visible when projected. One should minimize the number of slides with text only (I would strongly prefer no slides with text only, other than a conclusion slide at the end). Do not use schematics on black background. Do not use curves with thin lines or numbers on the axes with very small font that are hard to read. Results should be word-processed (no hand drawn / hand written materials / no scanned in).
- All project related materials are due electronically by email to me (mgh@gatech.edu) at the beginning of the class on the day that they are due. In the e-mail please identify name (of all people in the team), as well as on the first slide, so that I know who should get credit for the project. Projects handed in after this deadline and before the beginning of the next class lecture will be graded from 50% of the full grade. After the beginning of the next class, no project will be accepted. This policy is firm, so do not fall behind! The workload will not get any lighter later in the semester.
- Only one set of slides will be accepted per team. To help me archive the presentation files, please use this naming convention:

Team#_Draft1_ECE6414_S13.ppt , Team#_Presentation_ECE6414_S13.ppt , etc.

- Try to add a relevant title for each slide and add a brief description so that your slides would be self-explanatory. Also try to add one or two slides at the end as a conclusion.

Reading Assignments:

I will not keep track of class attendance. However, you are highly encouraged to attend all class and makeup sessions. Because there might be discussions in class that are not covered in the notes or textbooks.

Reading Assignments:

Reading assignments include sections of the textbooks, supplementary notes, literature search, and online articles that are relevant to the course topics. Class notes and supplementary notes, which topics may or may not be included in the textbook, will be posted on the class webpage and it is your responsibility to print them out and bring to the class with you. These materials will not be handed out during lectures. Students are responsible for both lecture material and reading assignments for the midterm, project, and final examinations.

Homework:

Homework will be assigned, as seen on the course webpage. The homework will include designs, hand calculations, and computer simulation problems. The homework will not be collected, but you are expected and highly encouraged to complete the problems because variations of those problems could be used in the exams.

Exams:

- There will be two closed book midterm examinations, each of 80 minutes duration.
- Rules of exam: One sheet of notes, last exam's sheet of notes, and a calculator.
- Each exam is cumulative: Every unit builds on all the previous units.
- Expect the unexpected: The exam will be over material covered in lectures (primarily), handouts, and in the textbook, but I reserve the right to make any / all problems not look like homework problems. I expect that you get the intuition of the key concepts from the homework. In the exam, you should be able to apply these concepts to slightly different problems.
- All grades become final one week after they are returned in class.

Missed Exam:

If you miss a midterm exam or do not attend your project presentation without a certified medical excuse or my prior approval, a zero will be averaged into your grade. Certified excuses and prior approval will be dealt with individually. Generally, only one makeup exam will be held at a designated time near the end of the semester and before the final exam. This means that there will be only one make-up test, independently from which exam/presentation you miss. Thus, the make-up test will be comprehensive. To request an excused absence, 1- write a formal letter to me (typeset), dated and signed, stating your specific request and the reason you are asking for an excused absence; 2- provide documentation supporting your request; 3- bring this letter and the documentation to me in person before the requested date (if an absence is foreseeable) or within

one week after the absence (if it is of unforeseeable nature), at which time your request will be discussed. Special cases will be dealt individually.

Academic Integrity:

It is the responsibility of the instructor to encourage an environment where you can learn and your accomplishments will be rewarded fairly. Any behavior which compromises the basic rules of academic honesty as described in the General Catalog will not be tolerated. It is the instructor's understanding that the student's signature on any test or assignment means that the student neither gave nor received unauthorized aid. For more information: http://www.osi.gatech.edu/plugins/content/index.php?id=31

Disabilities:

Reasonable accommodations will be made for students with verifiable disabilities. To qualify for these accommodations, students must register with Access Disabled Assistance Program for Tech Students (ADAPTS). For more information: http://www.adapts.gatech.edu/

Grading Policy:

Midterm-1	20%	A: 90 – 100	B: 70 – 89
Midterm-2	30%	C: 50 – 69	D: 40 – 49
Project	50%	F: 0 – 39	

Project Grading:	Draft-1	5%
	Draft-2	10%
	Layout quality/techniques	10%
	Simulation results	10%
	Circuit performance	10%
	Presentation	20%
	Final Paper	30%
	Group cooperation	5%

Auditing Criteria:

The ECE department does not grant any auditing credit. However, if you are interested in just sitting in the class, please contact me.

Course Schedule (Tentative):

Exam/Project	Date	Time
Project Draft 1	Tuesday 2/5/13	In class
Midterm 1	Tuesday 2/19/13	In class
Project Draft 2	Tuesday 2/26/13	In class
Design Review	Friday 4/5/13	4-6 pm
Midterm 2	Tuesday 4/16/13	In class
Post-layout	Friday 4/26/13	4-6 pm
Final Presentations	Tuesday 4/30/13	2:30 - 5:30pm
Final Papers	Friday 5/3/13	12 pm